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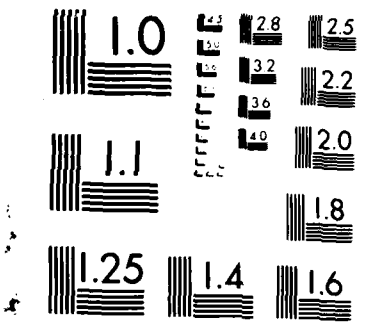

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DIGITAL PRE-PROCESSOR for the PORTABLE CHANNEL PROBER MEASUREMENT INSTRUMENT

Final Report
September 1986

Contract No. N00014-86-C-2161
(Stow Computer Project NRL01)

Prepared for

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19 ABSTRACT (*Continue on reverse if necessary and identify by block number*)

This document describes a Digital Pre-processor for the Portable Channel Prober Measurement Instrument being developed by the Naval Research Laboratory for use in experiments designed to characterize high frequency (HF) radio channels. This Digital Pre-processor is a digital signal processor designed and constructed by Stow Computer, 111 Old Bolton Road, Stow, MA 01775, (617) 897-6838. The Digital Pre-processor will be located at the receiver site of the channel probing experiment and is situated between the receiver and the microcomputer used for data recording and analysis. The Digital Pre-processor performs functions that cannot practically be performed by the general purpose microcomputer. The Digital Pre-processor converts the analog output of the receiver to digital data for processing, recording, and analysis. It performs digital signal
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processing on the data before recording or analysis by the general purpose microcomputer. It may perform data reduction to reduce the volume or rate of data. The Digital Pre-processor described is designed for portable use. It is small enough to be used on a table top or may be mounted in a standard equipment rack.

The Digital Pre-processor described is a versatile programmable data acquisition and signal processing instrument. Two identical data channels are provided for the in-phase and quadrature outputs of the coherent radio receiver used in the channel prober experiment. Analog to digital conversion is 12 bits precision and is done at a programmable rate which can exceed 250 kHz for each channel sampling both channels simultaneously. An input is provided for an external system coherent clock. Digital processing is done with a pair of Texas Instruments TMS32020 processors. A double buffer memory (swinging buffer) is used as a data memory and output buffer. A computer interface is provided to transfer data to a general purpose microcomputer for further analysis and recording. The Digital Pre-processor used the industry standard VME bus architecture for backplane interconnection.

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SECTION 1

INTRODUCTION

This document is a final report prepared by Stow Computer of Stow, Massachusetts for the Naval Research Laboratory upon completion of Contract number N00014-86-C-2161 for the design and construction of a Digital Pre-Processor for the Portable Channel Prober Measurement Instrument. The Digital Pre-processor described below is a subsystem of the Portable Channel Prober being developed by the Naval Research Laboratory for use in experiments designed to characterize high frequency radio communications channels. The Digital Pre-processor described is designed for portable use. It is small enough to be used on a table top or could be mounted in a standard equipment rack. The Digital Pre-processor will be located at the receiver site of the channel probing experiment and is situated between the receiver and the microcomputer used for data recording and analysis. The Digital Pre-processor performs functions that cannot practically be performed by the general purpose microcomputer. The Digital Pre-processor converts the analog output of the receiver to digital data for processing, recording and analysis. It performs digital signal processing on the data before recording or analysis by the general purpose microcomputer. It may perform data reduction to reduce the volume or rate of data.

The Digital Pre-processor is a versatile programmable data acquisition and signal processing instrument. It was designed, however, for a particular type of experiment which is reflected in the design. In the experiment a pseudo-random number sequence is transmitted. At the receiver

site the Digital Pre-processor converts the receiver output to digital values and stores the received sequence for processing by a general purpose microcomputer. Several received sequences may be integrated by adding corresponding samples before being sent to the microcomputer.

The experiment uses two different sequences. The Sounder Mode sequence is 255 bits and the transmitted pulse width is 8 usec with a 25% duty cycle. The received waveform can be integrated for 1,2,4, or 8 sequence lenghts. The received waveform is sampled at 32 us intervals. The sampling can be uniform or delayed by 4 usec between integrations. The Sounder Mode is used to get a preliminary characterization of the channel.

The Prober Mode uses a 2047 bit pseudo-random number sequence and is used to more accurately measure the channel. The transmitted pulse width is 1 usec with a 25% duty cycle. The received waveform is sampled at 4 usec intervals. The sampling can be uniform or delayed by .5 usec between integrations of 1,2,4 or 8 sequences.

1.1 Description

The Digital Pre-processor consists of two identical channels. Each channel processes one of the two quadrature (I and Q) baseband output signals from a coherent radio receiver. Each channel consists of an Analog to Digital Converter, an Integrator, and a Double Buffer Memory. Physically, the corresponding circuits for each channel are located on the same circuit board and share common control circuitry. The Digital Pre-processor is implemented using the VMEbus architecture which is an

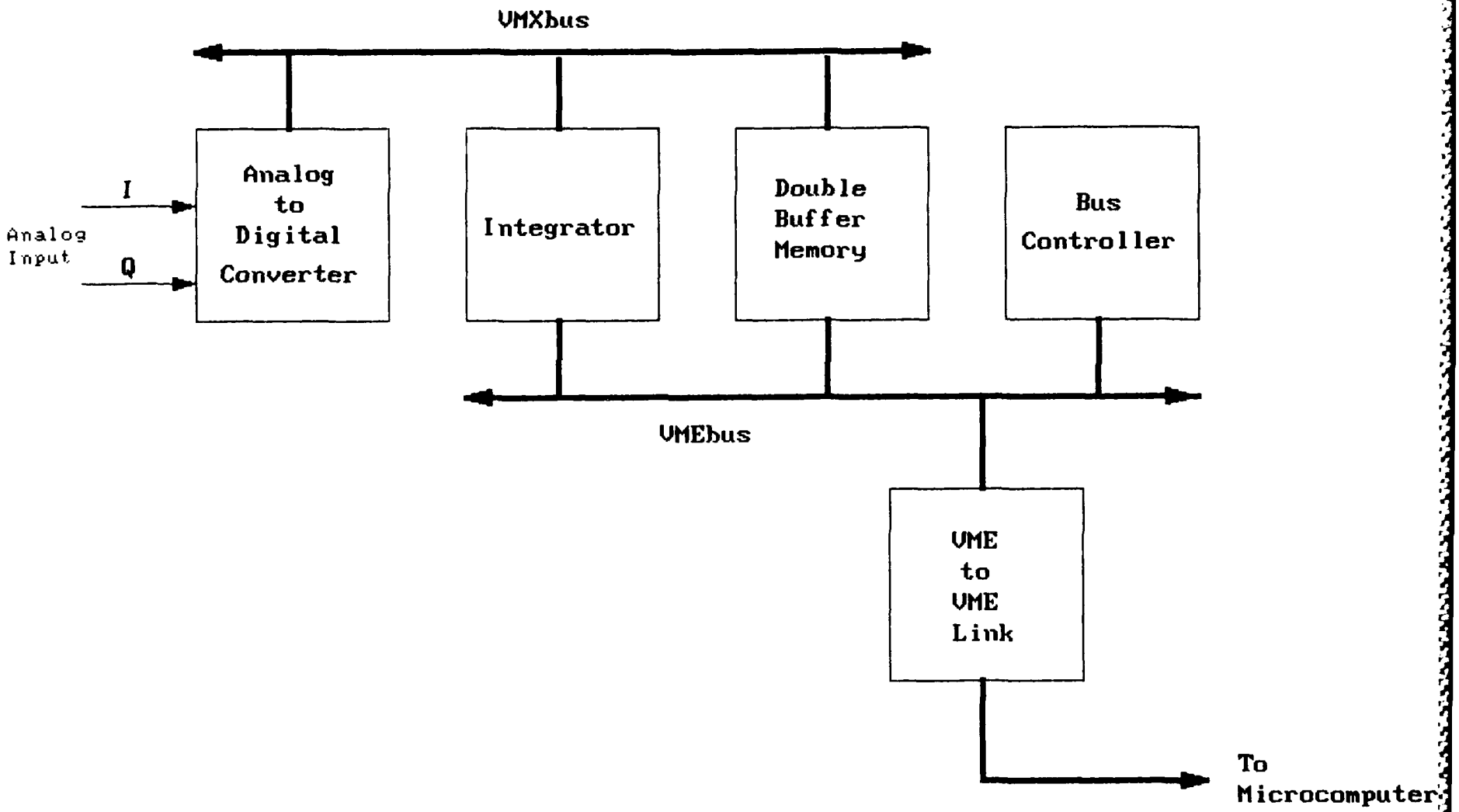


Figure 1-1 Digital Pre-processor

industry standard open architecture for the interconnection of high performance computing elements recognized by the IEEE and IEC. A double height VME circuit board is used for each function. A block diagram of the Digital Pre-processor is shown in Figure 1-1. A second bus based on the VMXbus, a VMEbus auxillary bus, is used as a local bus for data transfers between the components of the Digital Pre-processor. The bus controller module provides the required VMEbus system functions. A VMEbus to VMEbus link is provided to interface with a VMEbus based microcomputer. The following paragraphs briefly describe each of the components of the Digital Pre-processor. A more complete description of each of the major components is given in the following sections.

1.1.1 Analog to Digital Converter

The Analog to Digital Converter has two channels each with 12 bits precision and capable operation at a rate in excess of 250 kHz. The bipolar input voltage range is +/-5 volts. The Analog to Digital Converter is a slave device to the Integrator. The Analog to Digital Converter simply performs conversions on command. All mode differences are handled by the Integrator. During idle periods the integrator may strobe the Analog to Digital Converter in response to a request from the microcomputer for a sample to be used in setting the receiver AGC level. During data collection sampling is controlled by a coherent counter which is part of the Integrator and has been synchronized by an external Timing Module. The Analog to Digital Converter signals the Integrator when a conversion is complete. The I and Q channel data are sign extended to 16 bits and concatenated. The Integrator reads the output register of the Analog to Digital Converter over the VMXbus as a single

32 bit longword. The Analog to Digital Converter is described further in Section 2.

1.1.2 Integrator

The Integrator is the primary processing and control subsystem of the Digital Pre-processor. The Integrator controls the sampling of the Analog to Digital Converter, reads the samples, performs scaling, and sums the current samples with the corresponding samples of previous sequences to perform integration. The Integrator uses two Texas Instruments TMS32020 digital signal processors to perform identical processing on the two data channels. The two signal processors share a common program memory. In addition to the program memory the Integrator includes several registers and coherent counters that are accessed by the TMS32020's and are used to set the parameters of data collection. Parameters that are programmable via the coherent counters are sample rate, sequence length and integration. In addition, two coherent reference counters are provided so that two modes of data collection can be supported without resynchronizing with the external Timing Module. The program memory and registers are loaded via the VMEbus. Another register allows data samples to be read over the VMEbus for use in setting the receiver's AGC level. Data transfers from the Analog to Digital Converter and to and from the Double Buffer Memory are made over the VMXbus with the I and Q values concatenated to form 32 bit longwords. The Integrator uses the Double Buffer Memory both as temporary storage during data collection and as an output buffer for transmission of data to the microcomputer. The computational capabilities of the TMS32020 digital signal processors combined with the programmabiltiy of data collection parameters and the versatility of the VMEbus architecture make the Integrator

and the Digital Pre-processor a powerful tool for the collection and processing of data. The Integrator is described further in Section 3.

1.1.3 Double Buffer Memory

The Double Buffer Memory consists of two buffers which periodically switch function in a ping-pong fashon. At any time one buffer is available to the Integrator via the VMXbus for data collection and the other is accessable via the VMEbus for data transmission. The buffers switch function on command from the Integrator which sets a bit in a control register configuring the memory. The capacity of each buffer is 2048 32 bit longwords. Each buffer is sufficient to hold a 2047 bit sequence and an identification tag. The I and Q samples are concatenated into a single 32 bit longword to make better use of the available bus bandwidth than would two 16 bit transfers. The control register can be read over the VMEbus to check the status of the buffer. The Double Buffer Memory is further described in Section 4.

1.1.4 Parallel Interface

The parallel interface between the Digital Pre-processor and the Channel Prober's VMEbus based microcomputer is a commercially available product from VME Microsystems International Corporation model VMIDMAL. The interface can perform 32 bit transfers at a rate of 2 megabytes/second in single transfer mode. This rate provides a good margin over the Digital Pre-processor's maximum data rate of 1 megabyte/second. The VMIDMAL also has block mode and interrupt capabilities that may be used for future system enhancements.

1.1.5 System Controller

The System Controller is based on a Signetics SMVME1200 VMEbus Prototype Board. This board provides bus arbitration and other required VMEbus functions. A phase-locked loop is used to generate the VMEbus system clock, SYSCLK, from an external system coherent reference. SYSCLK is distributed on the VMEbus and is used by the Integrator for sample timing.

1.2 Physical Description

The Digital Pre-processor is self-contained comprising a cabinet and a chassis with a power supply and card cage. The chassis may be removed for rack mounting. The Digital Pre-processor in its cabinet is approximately 20" wide x 7.5" high x 20"deep. The approximate weight is 50 pounds.

1.3 Interface to the Channel Prober

1.3.1 Analog Inputs

- o Two Channels, I and Q, bipolar +/-5 volts
- o High impedance or optional terminating resistors
- o Rear panel BNC connectors

1.3.2 Coherent Clock

- o 1 mHz at TTL levels
- o Rear panel BNC

1.3.3 External Synchronization Input

- o TTL levels
- o Rear panel BNC

1.3.4 Control and Data Interface

- o Interface card in the microcomputer connected by two 64 conductor ribbon cables to a similar card in the Digital Pre-processor

SECTION 2

ANALOG to DIGITAL CONVERTER

The Analog to Digital Converter is a dual height VME circuit card with sample/hold and analog to digital converter modules for both the I and Q channels. The Analog to Digital Converter receives SAMPLE* commands from the Integrator, performs the conversion and asserts EOC* (end of convert). The Integrator reads the digital values for the I and Q channels over the VMXbus.

2.1 Analog to Digital Converter Description

The Analog to Digital Converter uses hybrid sample/hold and analog to digital converter modules manufactured by Datel. The ADC-810 analog to digital converter module used with the SHM-4860 sample/hold module is capable of performing 12 bit conversions at a rate greater than 250 kHz. The analog to digital converter module is configured for bipolar input of +/-5 volts. Potentiometers allow adjustment of the gain and offset of each channel. The sample/hold module has a high input impedance and provision is made for an optional terminating resistor if required. The output of the analog to digital converter modules is clocked into a register at the end of the conversion. A new conversion can be started before the previous value is read without loss of data. The I and Q values are sign extended from 12 to 16 bits and read as a single longword by the Integrator over the VMXbus.

SECTION 3

INTEGRATOR

The Integrator, NRL0101, is a dual height VME circuit that is the primary processing and control subsystem of the Digital Pre-processor. The Integrator utilizes two digital signal processing microprocessors configured to process two data channels in parallel. The two signal processors share a common program memory and are synchronized to run in lock step processing the two channels identically. Coherent counters are used as timers to control data collection. The parameters of the data collection are determined by the moduli of these counters and are programmable via I/O registers.

The data path is primarily over the VMXbus. Program memory and control registers are accessed over the VMEbus. A register is provided to supply input samples over the VMEbus for setting the receiver's AGC level. Interfaces are provided for the Analog to Digital Converter and for external synchronization. The VMEbus system clock, SYSCLK, is assumed to be a coherent clock derived from an external standard.

3.1 Integrator Block Diagram

Figure 3-1 is a block diagram of the Integrator. Three primary data paths are evident from the diagram. The VMXbus is the interface to the Analog to Digital Converter and the Double Buffer Memory and is used primarily for processing samples. The VMEbus is used to load the program RAM and control registers and to read the input samples used in setting the receiver's AGC level. The internal bus

connects the signal processors, program memory, registers, and the VMEbus interface.

3.2 Integrator Design Description

The Integrator uses two Texas Instruments TMS32020 digital signal processing microprocessors to perform identical operations on the I and Q data channels. The two processors share a common program memory. The TMS32020s run on their own 20 mHz clock which is not coherent with the system clock. The TMS32020s interact asynchronously with the VMXbus which is asynchronous by definition and also with the program RAM and various I/O registers. The TMS32020s must, however, maintain synchronism with each other and appear to the rest of the circuitry as a single entity. This synchronism is achieved by suppling the 20mHz from a common oscillator and then supplying a sync signal to force the internal clock of each processor to the same phase. To compensate for slight differences between the two processors all output control signals are combined to correspond to the slower timing of the two processors and all inputs to the faster.

The VMEbus interface allows 16 bit transfers between the VMEbus and the control registers and program RAM. It is used by the microcomputer to download programs and to set experiment parameters. Since the VMEbus interface shares the internal bus with the signal processors it must receive a DMA grant before completing a transfer. Since the signal processors are operating under real time constraints during data collection the VMEinterface would normally be used only during idle times. The VMEbus interface uses PLD's (programmable logic devices) as combination address

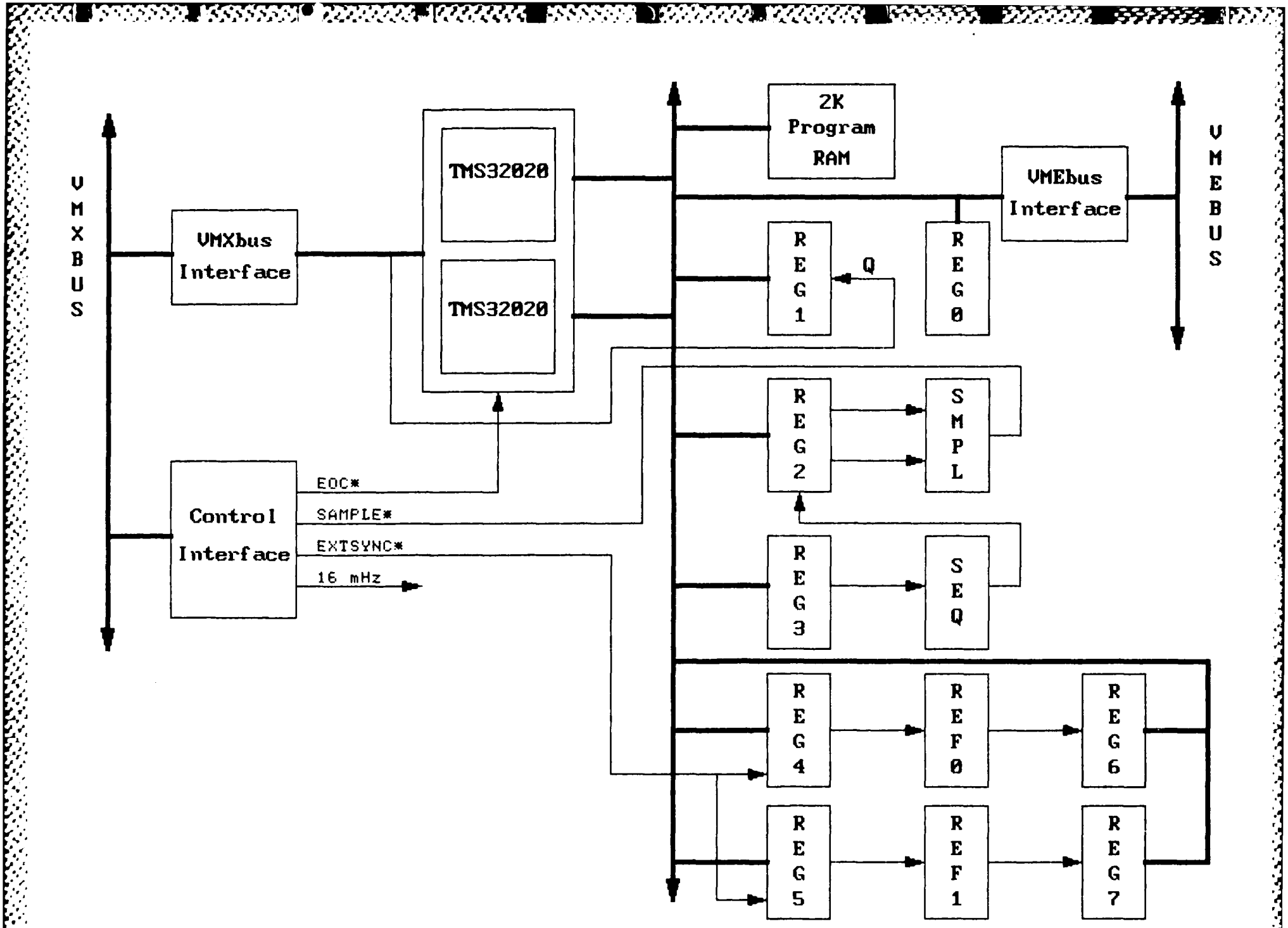


Figure 3-1 Integrator

receivers and decoders. A 68172 bus controller is used to interface the internal strobes to the VMEbus protocol.

The VMXbus interface is the bus master. A tapped delay line is used to generate the signals required from those available from the signal processor. Data transfers are 32 bits wide with the upper 16 bits carrying the I channel value and the lower 16 bits carrying the Q channel value.

The first 32 locations of the program RAM are used for interrupt vectors. The remainder is used for signal processor programs. Programs will not generally be executed directly from the program RAM but will be copied into the signal processors' internal RAMs for faster program execution. The program RAM is 2048 x 16 bits of 70ns static RAM.

The eight registers and four counters shown are described in a later section.

3.3 Typical Operation

After power-up the signal processors are held in an inactive state. The program RAM is loaded from the microcomputer over the VMEbus to VMEbus link. The registers are loaded with the parameters for data collection. The reference counters are synchronized by the external Timing Module. The signal processors are reset by setting and clearing a bit in the control register. The first program executed is a loader program which copies the program RAM

into internal RAM and branches to an idle loop waiting for requests for AGC samples and testing the ACTIVE* bit in the control register. When the AGC bit is detected the Integrator strobes the Analog to Digital Converter and writes the I and Q samples to a register for the microcomputer to read over the VMEbus. When the ACTIVE* bit is detected the processor jumps to a loop to process the first sequence. After the first sequence has been stored in memory the program jumps to an integration loop and completes the frame. At the end of the frame the program jumps back to the first sequence loop. Processing continues until the Integrator is interrupted by the microcomputer and the ACTIVE* bit set to idle. The RAM and registers can now be loaded for a different mode of data collection. It is not necessary to resynchronize the reference counters.

3.4 Typical TMS32020 Software

The following is TMS32020 assembly language code for the integration loop. This loop must execute in less than the 4 usec sampling period in the Prober mode. Execution time has been calculated to be 3.8 usec.

```
BIOZ    Branch on BIO pin zero
        [Test for A/D done]
B       Branch back
        [Form wait loop]
LAC     Load accumulator with shift
        [Read A/D and scale]
ADD     Add
        [Read previous sample from memory
         and add to accumulator]
SACL    Store accumulator low 16 bits
        [Write new value to memory and
         increment address pointer)
CMPR    Compare register
        [Compare address pointer with
         upper limit]
BBZ     Conditional branch
        [If pointer OK branch to BIOZ]
```

LAR	Load register [Else load initial value]
B	Unconditional branch [Branch to BIOZ]

3.5 Description of Registers

3.5.1 Register 0; Control Register

Register 0 is an eight bit register primarily written from the VMEbus and read by the TMS32020s. Bits 15-7 are ignored on writes and read as 1's.

Bit 0 ACTIVE* 1 puts Digital Preprocessor into IDLE state in terms of data collection.
0 initiates data collection.
Bit 1 AGC* 1 AGC sampling inactive.
0 initiates taking of samples to set the AGC level if the processor is in the IDLE state in terms of data collection.
Bits 2,3 not used
Bits 4,5,6 INT0*, INT1*, INT2*
1 inactive
0 causes TMS32020 to be interrupted at the level selected.
Bit 7 SWRS* 1 inactive
0 causes the TMS32020s to be reset

3.5.2 Register 1; AGC Samples

Register 1 is a sixteen bit register primarily written by the TMS32020 and read by the VMEbus. Bits 7-0 transfer 8 bits of Q data. Bits 15-8 transfer 8 bits of I data. Bits 15-8 can be read and written from the VMEbus, bits 7-0 can be read but not written from the VMEbus.

3.5.3 Register 2; Sample Timing

Sixteen bit register primarily written by the VMEbus. The register output sets the modulus of the sample rate divider. The register can be read and written by the TMS32020 or by the VMEbus. This is primarily intended for diagnostic purposes. Bits 7-0 are determine the time between samples within a frame. Bits 15-8 determine the time between the last sample of one frame and the first sample of the next frame.

3.5.4 Register 3; Sample Counter

Sixteen bit counter primarily written by VMEbus. The output sets the modulus of a counter that counts the number of samples taken in a frame. Bits 15-0 contain the one's complement of the total number of samples in a frame (samples x integration). This register is meant primarily to be written to by the VMEbus. It may, also, be read and written from the VMXbus primarily for diagnostic purposes.

3.5.5 Register 4; Reference Counter 0

Modulus Register 4 sets the modulus of one of the two coherent reference counters. Register 4 is primarily written by the VME bus although it can be read and written from both buses. Register 4 is 8 bits wide and sets the upper 8 bits of the 12 bit reference counter to the one's complement of the length of the reference sequence. The four least significant bits are hardwired to 0001.

3.5.6 Register 5; Reference Counter 1

Modulus Register 5 sets the modulus of reference counter 1. Register 5 is identical to Register 4 except for its address.

3.5.7 Register 6: Reference Counter 0 Sample

Register 6 is used to sample reference counter 0 when the Integrator commands the Analog to Digital Converter to sample the receiver output. Register 6 is 16 bits wide and is primarily read by the TMS32020 although it can also be read from the VMEbus. Register 6 cannot be written either from the VMEbus or by the TMS32020.

3.5.8 Register 7; Reference Counter 1 Sample

Register 7 is used to sample reference counter 1. Register 7 is identical to Register 6 except for its address.

3.6 Description of Counters

3.6.1 Sample Divider

The sample divider is a synchronous 8 bit counter which runs on a system coherent 4 mHz clock. The sample divider divides the 4 mHz clock to the input sampling rate and strobes the Analog to Digital Converters. The modulus of the counter is set from register 2. Register 2 holds two moduli, one is used to space the samples within a frame and the other is used to space the frames. The modulus to be used is selected using a multiplexer controlled by the output of the sample counter, LAST. The sample divider is

held at its preset value when the Digital Preprocessor is in the IDLE state. The register value required to set the modulus of the counter is determined as follows: Express the sampling period in 250ns increments as an 8 bit binary number, subtract 1 and take the one's complement.

For example in the Prober Mode:

0001 0000	4 usec in units of 250 ns
0000 1111	Subtract 1
1111 0000	Complement

For the Sounder Mode:

1000 0000	32 usec in units of 250 ns
0111 1111	Subtract 1
1000 0000	Complement

The interval between frames is determined in the same manner. This value is stored in the 8 MSB's of register 2. In the Prober Mode, for example, to wait 4.5 usec between the last sample in one frame and the first sample of the next:

0001 0010	4.5 usec in 250 ns increments
0001 0001	Subtract 1
1110 1110	Complement

Another example for 40 usec spacing between frames in Sounder Mode:

1010 0000	40 usec in 250 ns units
1001 1111	Subtract 1
0110 0000	Complement

To sample at 4 usec intervals and have 4.5 usec between frames load register 2 with: 1110 1110 0110 0000 To sample at 32 usec intervals with 40 usec between frames load register 2 with: 0110 0000 1000 0000. For uniform sampling store the same value in the upper and lower half of register 2. For example: 1111 0000 1111 0000 results in uniform 4 usec sampling.

3.6.2 Sample Counter

The sample counter counts the number of samples strobed by the sample divider and generates LAST coincident with the last sample of the frame. The sample counter is a sixteen bit counter. It is clocked by the 4 mHz system clock gated by SAMPLE. The modulus of the counter is set by register 3. The value to be loaded into register 3 is determined by writing the number of samples in a frame as a sixteen bit binary number, subtracting one and taking the one's complement. The number of samples in a frame is equal to the number of samples in a sequence multiplied by the number of sequences to be integrated.

In Sounder Mode:

0000 0000 1111 1111	255 sample sequence with no integration
0000 0000 1111 1110	Subtract 1
1111 1111 0000 0001	Complement

In Prober Mode with an Integration of 4:

0001 1111 1111 1100	2047 sample sequence integrated for 4 sequences
0001 1111 1111 1011	Subtract 1
1110 0000 0000 0100	Complement

3.6.3 Reference Counters

Two coherent reference counters are provided. The coherent counters are used to maintain the the timing relationship between the samples of the received waveform and a local reference independent of any processing delays. An external synchronization signal is used to synchronize the counters with an external reference. Having two counters allows switching between two modes without resynchronizing. The two counters are identical. The software must know which counter is relevant to the current mode of operation. The modulus of reference counter 0 is set by register 4. Reference counter 0 is sampled by register 6. The modulus of reference counter 1 is set by register 5. Reference counter 1 is sampled by register 7. The reference counters are 12 bit counters and are free running on the 4 mHz coherent clock. Only the 8 MSB's of the 12 counter bits are set by the registers. The four LSB's are wired to 0001. To determine the value to be loaded into the register (4 or 5) write the sequence length as a 12 bit binary number, subtract 1, and take the one's complement. The 8 MSB's are used to set the modulus of the counter the 4 LSB's should be 0001.

For the Sounder Mode:

```
0000 1111 1111  Sequence length 255
0000 1111 1110  Subtract 1
1111 0000 0001  Complement
     1111 0000  Value to be loaded into register 4
```

For the Prober Mode:

```
0111 1111 1111  Sequence length 2047
0111 1111 1110  Subtract 1
1000 0000 0001  Complement
     1000 0000  Value to be loaded into register 5
```

SECTION 4

DOUBLE BUFFER MEMORY

The Double Buffer Memory, NRL0102, is a double height VME circuit with 16K bytes of data RAM. The RAM memory is organized as two buffers of 2048 x 32 bit words. The Double Buffer Memory has interfaces to the VMEbus and the VMXbus. At any time one buffer is connected to the VMXbus and the other is connected to the VMEbus. The buffer connected to the VMXbus is used as a data memory by the Integrator for the storage of input samples and of partial sums during integration. Sixteen bit samples from the I and Q channels are concatenated to form 32 bit longwords for transfer over the VMX and VME buses. When the integration of input sequences is complete the buffers are exchanged. The integrated input samples can now be read over the VMEbus to be transfered to the microcomputer for further processing and an empty buffer is available to the integrator for storage of the next input sequence. The orientation of the buffers is controlled by one bit of an octal register that can be read and written from the VMXbus. The control register can be read from the VMEbus but not written. The seven remaining bits of the control register are available and can be used to pass status information from the VMXbus to the VMEbus.

4.1 Double Buffer Memory Block Diagram

Figure 4-1 is a block diagram of the Double Buffer Memory. The control register switches the two 2048 x 32 bit buffer memories "A" and "B" between the VMXbus and VMEbus interfaces. Each buffer holds up to 2047 16 bit I samples

and a tag and 2047 16 bit Q samples and a tag concatenated to form 32 bit longwords. The control register can be read and written from the VMXbus and is read-only from the VMEbus. In addition to the bit controlling the orientation of the buffers, the control register has seven bits available for use in passing information between the VMX and VME buses.

4.2 Circuit Description

The Double Buffer Memory circuitry will be described in terms of the functional blocks shown in the block diagram, Figure 4-1. The four blocks described below are: the VMXbus Interface, the VMEbus Interface, the identical Buffer Memories "A" and "B", and the Control Register.

4.2.1 Double Buffer Memory VMXbus Interface

The VMX interface is designed to provide fast access to the memory from the VMXbus. When the Integrator is integrating input sequences it must perform a read and a write operation to the Double Buffer Memory during each sample period. It is important that the Double Buffer Memory add as few wait states as possible to the TMS32020 read or write cycle.

High speed PLD's (programmable logic devices) are used as combination bus receivers, address registers, and address decoders. The same PLD's serve both the RAM memory and the control register. A tapped delay line is used to sequence the enables required for a read or write operation and finally to assert the VMXbus acknowledge signal ACK* to end the cycle. ACK* is asserted approximately 100 ns after the

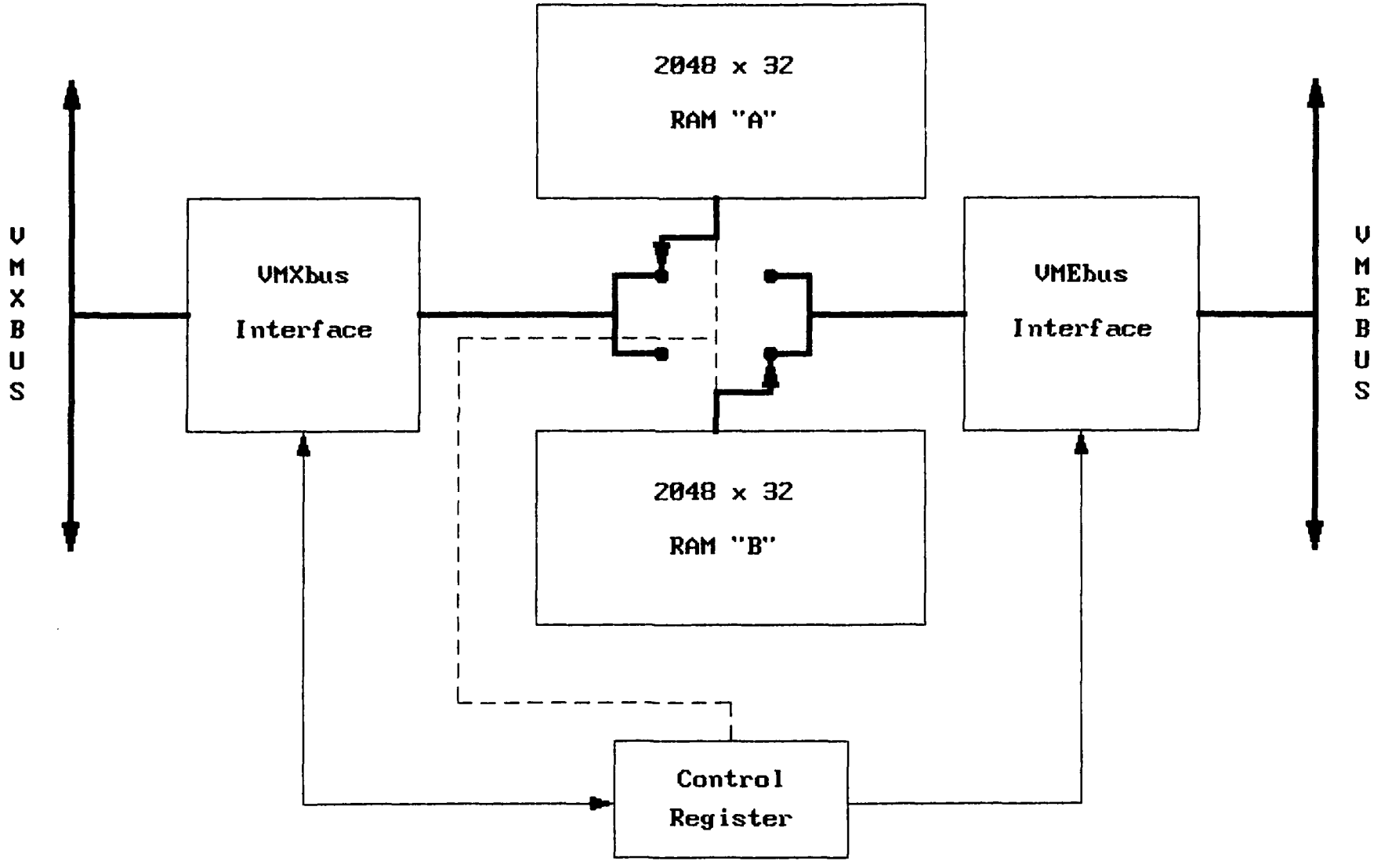


Figure 4-1 Double Buffer Memory

Double Buffer Memory receives a data strobe from the Integrator.

4.2.2 VMEbus Interface

The VMEbus interface uses PLD's (programmable logic devices) as address receivers, buffers, and decoders. A 68172 bus interface provides the interface between the local decoding and the VMEbus protocol.

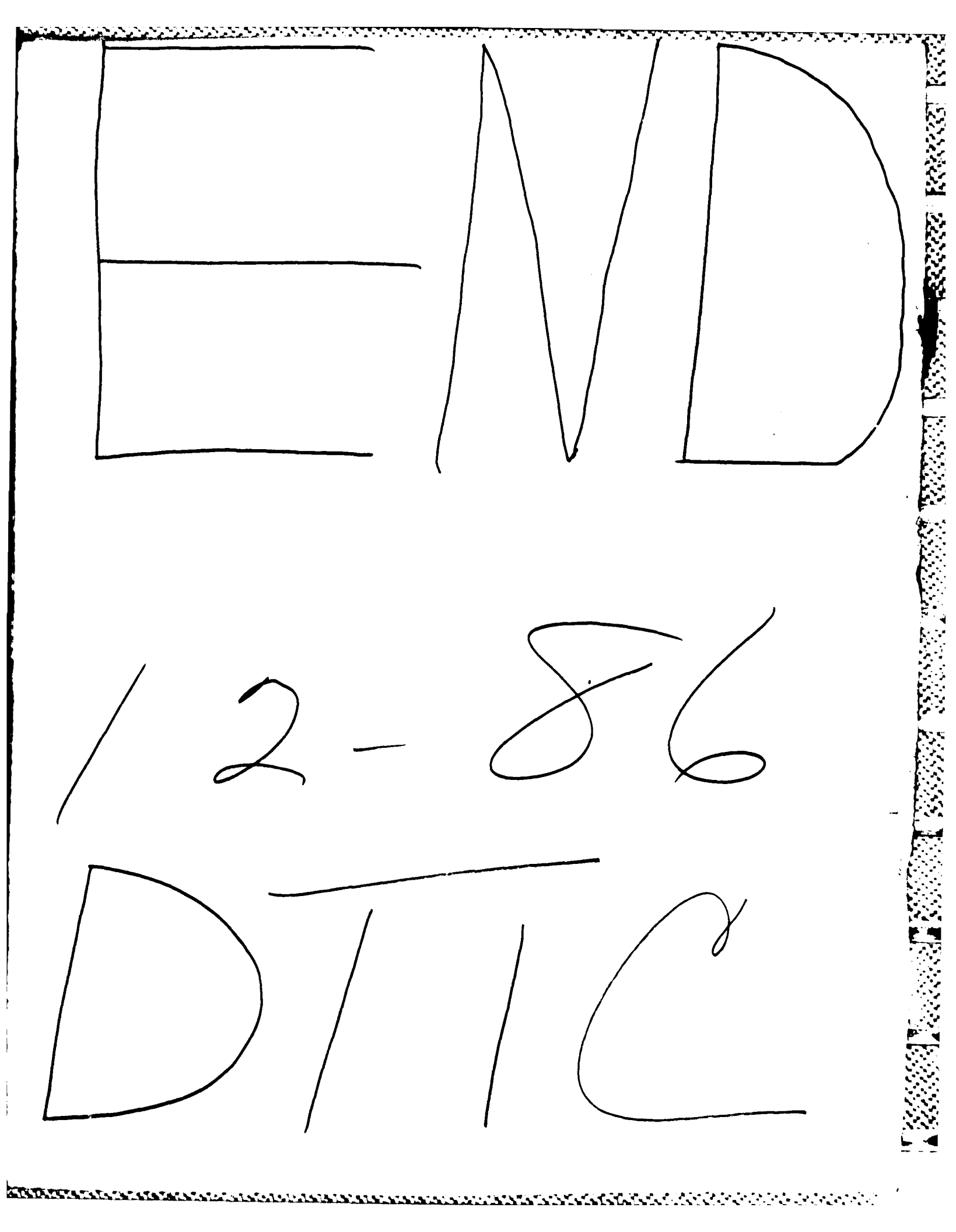
4.2.3 RAM Memories "A" and "B"

The 2048 x 32 bit data memories are identical. Each memory consists of four 9128 70ns 2048 x 8 bit RAM's. The address and control inputs are multiplexed between the two bus interfaces. Two sets of transceivers, one connected to each bus, are used to buffer the data. The proper transceiver is enabled by control signals from the multiplexer.

4.2.4 Control Register

The Control Register consists of an octal registered transceiver that can be read and written from the VMXbus and an octal latch that allows the register to be read from the VMEbus. The latch is necessary on the VMEbus side since it would be possible to violate the bus specifications if the register contents were changed from the VMX side at the same time they were being read from the VME side.

The LSB of the register controls the orientation of the buffers. If the LSB is 1 buffer A is connected to the VMEbus interface. The remaining 7 bits of the register can be used to pass status information. The Control Register is connected to bits DB23-DB16 of the VMXbus and bits D07-D00 of the VMEbus. This cross connection is for diagnostic purposes.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